



Intel PC133 SO-DIMM Validation Specification for Intel Mobile Chipset Based Platforms

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Intel Corporation

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REVISION HISTORY

Revision	Draft/Changes	Date
0.5	Initial draft	10/3/00
0.6	System validation section update	10/16/00
0.8	SO-DIMM system validation functionality testing update	11/23/00
0.9	Created section 4.1 SO-DIMM validation process and sample requirement. Updated section 4.2 SO-DIMM validation test flow. Removed signal integrity test requirement in section 4.0	4/20/01
1.0	Minor edits	5/1/01

1.0 VALIDATION OVERVIEW

The objective of the Intel PC133 validation program is to verify 133Mhz SDRAM compliance to the Intel PC133 specification and the performance of SO-DIMM modules in Intel reference systems, so as to provide a guidance of memory compatibility to Intel chipsets. The validation is conducted at two levels: component and system level. Intel will publish a list of validated PC133 SDRAM devices and SO-DIMM modules on the web page.

Component level validation consists of device AC/DC/Functional tests and parasitic characterization. Device AC/DC/Functional tests include testing of critical parameters: tsi, thi, toh, tac, Vol, Voh, Iol, Ioh as well as Vcc and Vss clamp and I/O buffer I-V characteristics, while device parasitic characterization examines parasitic capacitance of input pins, data pins and clock pins.

System level validation verifies SO-DIMM module's functionality and compatibility on Intel reference platforms over specification ranges with industry standard and Intel specific test software.

2.0 Tests and Sample Requirements

2.1 Component tests

2.1.1 AC/DC and functional test conditions

Device AC/DC characteristics and functionality are tested to the PC133 specification limits as listed in [Table 1](#)

Table 1. AC/DC/Functional test conditions

Vdd	Vddq	Tc (device case temperature)
3.0V	3.0V	85C
3.6V	3.6V	85C
3.0V	3.0V	0C
3.6V	3.6V	0C

2.1.2 AC/DC and functional test program flow

The DC electrical and AC timing tests are conducted on HP83000 or equivalent automatic testers. A list of patterns are executed to confirm the device functionality and performance. The test program flow is summarized and described in [Table 2](#).

Table 2. AC/DC/functional test program flow

SEQUENCE	TEST	DESCRIPTION
1	Power up	Device power up and initialization

Table 2. AC/DC/functional test program flow

SEQUENCE	TEST	DESCRIPTION
2	Functional tests	March, March L/R, DQM patterns. Pass/fail at 133Mhz as well as at 100Mhz to insure PC100 compatibility.
3	Tac / Toh	Data set up and hold time. March pattern. Measured at 12pf tester load and the result converted to 50pf spec load
4	Tsi / Thi	input set up and hold time March and DQM patterns
5	Vih / Vil	Input voltage high / low March/DQM patterns at relaxed timing
6	Iccac	Active Icc. All banks open, ping-pong reads, BL=4, Measured at Vcc power supply
7	Ioh / Iol	DC test I/O buffer I-V characteristics Write FF for Ioh, 00 for Iol, then loop on read. Force voltage, measure current on DQ pins after settling time of 1us. For VDD = 3.45V, step forcing voltage from 3.45V to 0V with 0.2V interval. For VDD = 3.0V, step forcing voltage from 3.0V to 0V with 0.2V interval.
8	Vcc / Vss clamp	DC test Vcc / Vss clamp characteristics VCC CLAMP test: Force voltage, measure current on CLK, CKE, CS, DQM, and DQ pins after settling time of 10 ms. For VDD = 3.6V, step forcing voltage from 3.6V to 5.6V with 0.2V interval. For VDD = 3.0V, step forcing voltage from 3.0V to 5.0V with 0.2V interval VSS CLAMP test: Force voltage, measure current on CLK, CKE, CS, DQM, and DQ pins after settling time of 10 ms. For VDD = 3.6V, step forcing voltage from 0V to -2V with 0.2V interval. For VDD = 3.0V, step forcing voltage from 0V to -2V with 0.2V interval
9	END	

Device speed is tested at CL=3 or CL=2 depending on incoming device validation request. Intermediate speed is not tested.

2.1.3 Parasitic test

Device parasitic capacitance is characterized with a HP capacitance meter (Max freq. > 1Mhz). DUT is interfaced to test probe through a test fixture to allow ease of probing. The extra capacitance introduced by the test fixture is characterized and extracted from the final results. More information regarding detailed measurement set up is available from Intel.

The parasitic measurements are conducted under the conditions listed in [Table 3](#)

Table 3. Parasitic test conditions

Parameter	Value
Test Frequency	1Mhz
Probe Bias	1.4V with 200mV AC swing
Vcc	3.3V
Temperature	Room temperature

2.2 SO-DIMM System tests

SO-DIMM module's functionality and compatibility are tested on Intel reference platforms with industry standard and Intel specific test software. The test conditions are specified in [Table 4](#). SO-DIMM modules must be assembled with validated PC133 SDRAM components as listed on Intel web page: <http://developer.intel.com/technology/memory/pc133sdram/valid/pc133sdram.htm>

System level validation consists of memory SPD check, memory power up test (power cycling), power management test (S3) and functionality test.

Table 4. System test conditions

Corner	Vcc	Ambient temperature	System loading
1	3.0V	55C	Heavy/light in X-X config
2	3.6V	55C	Heavy/light in X-X config
3	3.0V	25C	Heavy/light in X-X config
4	3.6V	25C	Heavy/light in X-X config

For more details about system level tests, please refer to “[System Level Validation of SO-DIMM Modules](#)” on [page 13](#).

2.3 Validation sample requirements

Minimum validation sample requirement is summarized in [Table 5](#). SDARM submitted must pass supplier in-house components testing. SO-DIMM modules must be built with validated PC133 SDRAMs as listed on Intel web page (<http://developer.intel.com/technology/memory/pc133sdram/valid/pc133sdram.htm>) and pass in-house system testing.

Table 5. Minimum validation sample requirement

Validation Type	DRAM AC/DC/Functional	DRAM Parasitic	System test
Sample Requirement	3 devices per configuration per density	2 devices per configuration per density	8 SO-DIMMs per configuration per density

Table 5. Minimum validation sample requirement

Validation Type	DRAM AC/DC/Functional	DRAM Parasitic	System test
Recommended Data from Suppliers	Characterization data at Tcase = 0C, 85C and Vcc=3.0V, 3.6V, for min. of 2 devices	Parasitic data at room temperature for min. 1 device	DRAM pass Intel validation SO-DIMM pass factory system testing

3.0 PC133 Component Specification Validation

3.1 DC/AC/Functional validation

3.1.1 DC Tests

DC parameters are tested to Intel PC133 specification as shown in [Table 6](#). Functional tests are performed with various patterns at different input voltages to determine compliance to spec.

Table 6. D.C parameter tested

Symbol	Parameter	Condition	Min	Max	Units	Notes
Iccac	Icc active	All banks open, initialize solid 1 and 0 pattern, ping-pong reads, BL=4, Measured at Vcc power supply		140/165 185	mA	16M/64M 128M/256M

NOTE: No Activate or Precharge currents should be included in the Iccac value.

3.1.2 AC Tests

AC parameters are tested to Intel PC133 specification as shown in [Table 7](#). Functional tests are performed with various patterns at different input voltages.

Table 7. AC parameter tested

Symbol	Parameter	Condition	Min	Max	Units	Notes
Vih	Input High Voltage	Functional pass/fail	2.0	VDDQ+2.0	V	
Vil	Input Low Voltage	Functional pass/fail	VSSQ – 2.0	0.8	V	

AC timing parameters listed in [Table 8](#) are tested under the conditions specified in section 2.1.1. Test result must meet Intel PC 133 specification limits. Functional tests will be performed at 133Mhz and 100Mhz to guarantee device compatibility with PC100.

The correlation between load condition of HP83000 tester and that of PC133 specification condition are thoroughly investigated. A correction factor of 0.7ns and 0.6 ns is determined for Tac and Toh respectively. For a more detailed experiment report, see Appendix B.

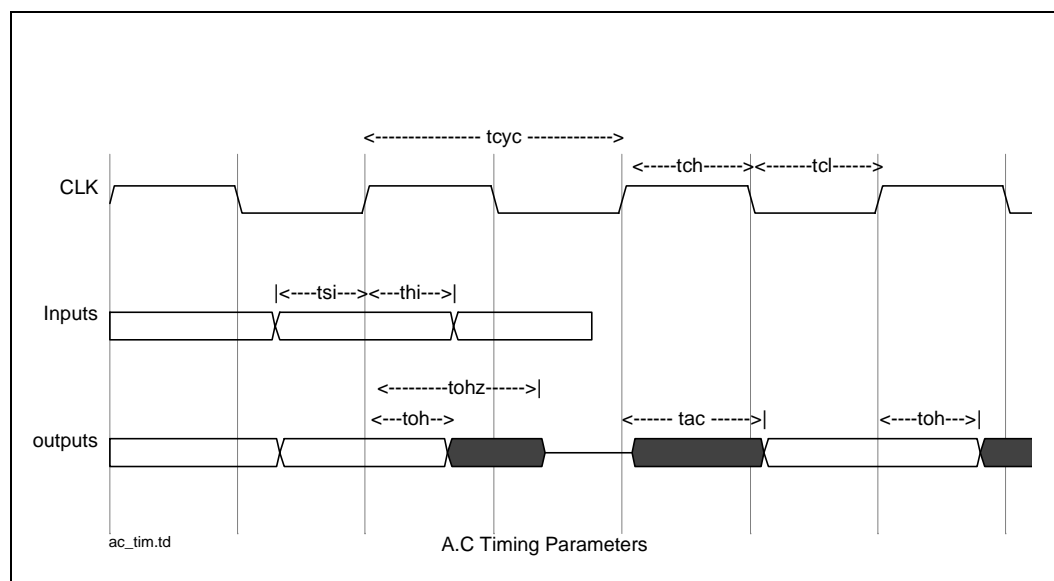
Table 8. 133/100/66 MHz AC Timing Parameters For $C_L=2$ and 3

Parameter	Symbol	Speed Grade 66 MHz		Speed Grade 100 MHz		Speed Grade ¹ 133MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Input Setup Times	Tsi	3		2		1.5		ns	
Input Hold Times	Thi	1.5		1		0.8		ns	
Output Valid From Clock	Tac		9		9		5.4	ns	
Output Hold From Clock	Toh	3		3		3		ns	Note 1
RAS# Active Time	Tras	5		5		6		Tclk	Functional test Note 2
Activate to Command Delay (RAS# to CAS# Delay)	Trcd	2		3/2		3/2		Tclk	Functional test Note 2
RAS# Precharge Time	Trp	3/2		3/2		3/2		Tclk	Functional test Note 2
Clock	Clk	3/2		3/2		3/2			Functional test Note 2

NOTE:

1. For 133MHz, either 3.0ns @ 50pF needs to be met with I/V curve, or 1.8ns @ 0pF needs to be guaranteed.
2. The parameter needs to be retested @ 100MHz to guarantee compatibility with PC100.

Figure 1. A.C Timing Parameters

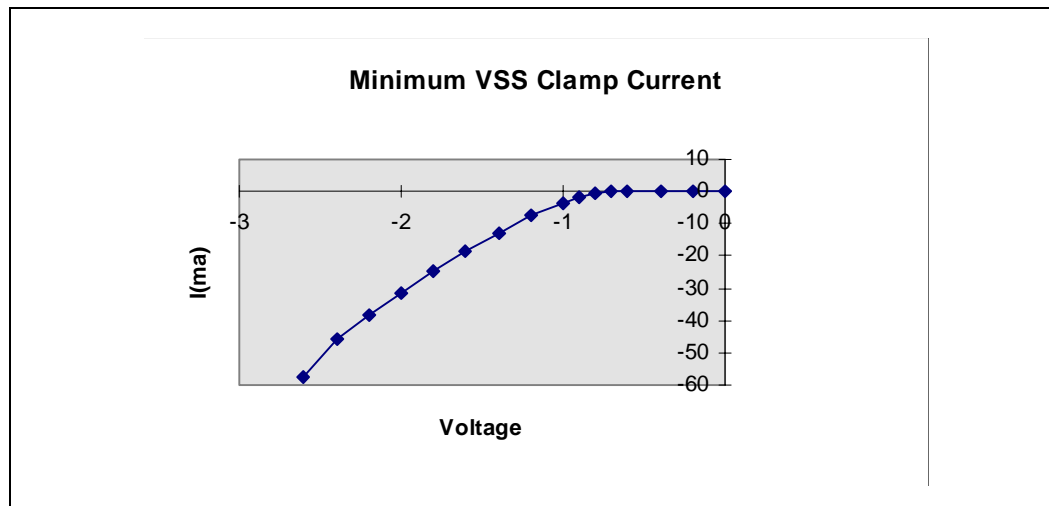


3.1.3 I/V Characteristics for Input and Output Buffers

3.1.3.1 Vss and Vcc clamp characteristics

Vss and Vcc clamp characteristics are tested for CK, CS, DQMB, DQ and CKE pins and are described in Figure 2 and Figure 3. Table 9 and Table 10 list the maximum (minimum in absolute value) and minimum required current levels at respective Vss and Vcc.

Figure 2. SDRAM VSS Clamp Characteristics



NOTES:

1. Required for CK, CS, DQMB, DQ and CKE pins.
2. This data is referenced to the ground.
3. Must meet the temperature and voltage range specified above.
4. This drawing is not to scale. Comparisons should be made to the data table provided.

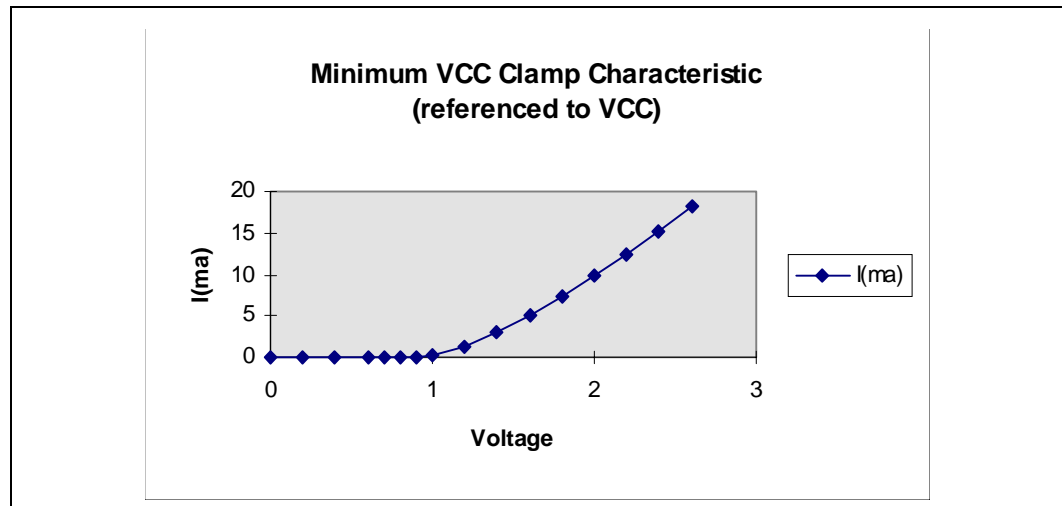
Table 9. Data Points For Figure 2

VSS	I (mA) (Max)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.65
-1.2	-7.57
-1	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05

Table 9. Data Points For Figure 2

-0.6	0
-0.4	0
-0.2	0
0	0

Figure 3. SDRAM Vcc Clamp Characteristics



NOTES:

1. Required for CK, CS, DQMB, DQ and CKE pins.
2. This data is referenced to the VCC voltage.
3. Must meet the temperature and voltage range specified above.
4. This drawing is not to scale. Comparisons should be made to the data table provided.

Table 10. Data Points For Figure 3

VCC	I(ma) (Min)
2.6	18.31
2.4	15.3
2.2	12.48
2	9.83
1.8	7.35
1.6	5.06
1.4	3.02
1.2	1.34
1	0.23
0.9	0
0.8	0

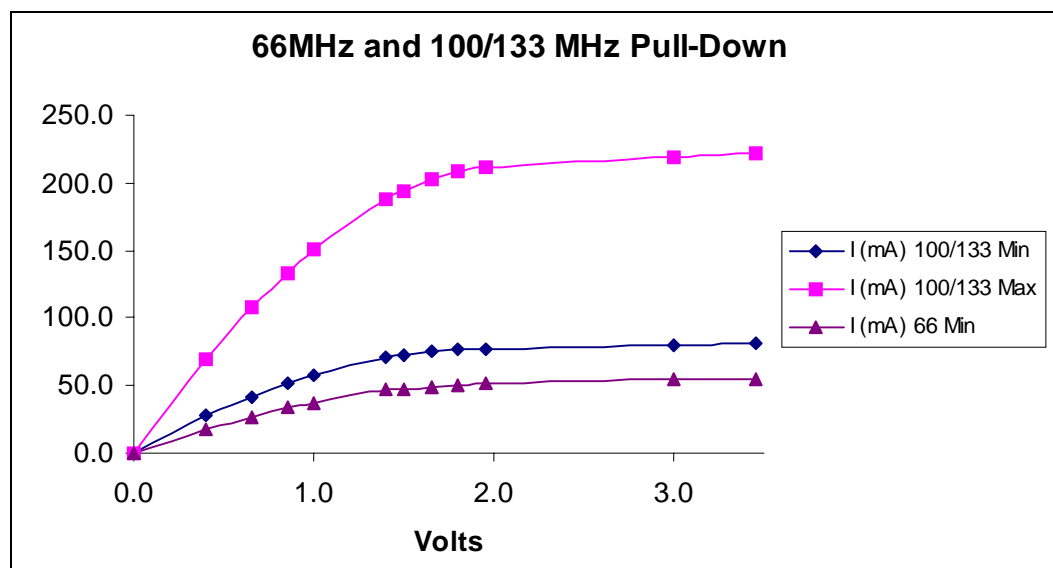
Table 10. Data Points For Figure 3

0.7	0
0.6	0
0.4	0
0.2	0
0	0

3.1.3.2 I/O Buffer Characteristics

I/O buffer pull-down and pull-up characteristics are described in Figures 4 and 5. I-V characteristics are determined for all DQ pins in the voltage range specified in Table 11 and Table 12. The test results must be within the specification ranges.

Figure 4. SDRAM DQ Output Buffer Pull-Down Characteristics (Vcc= 3.0-3.45V)



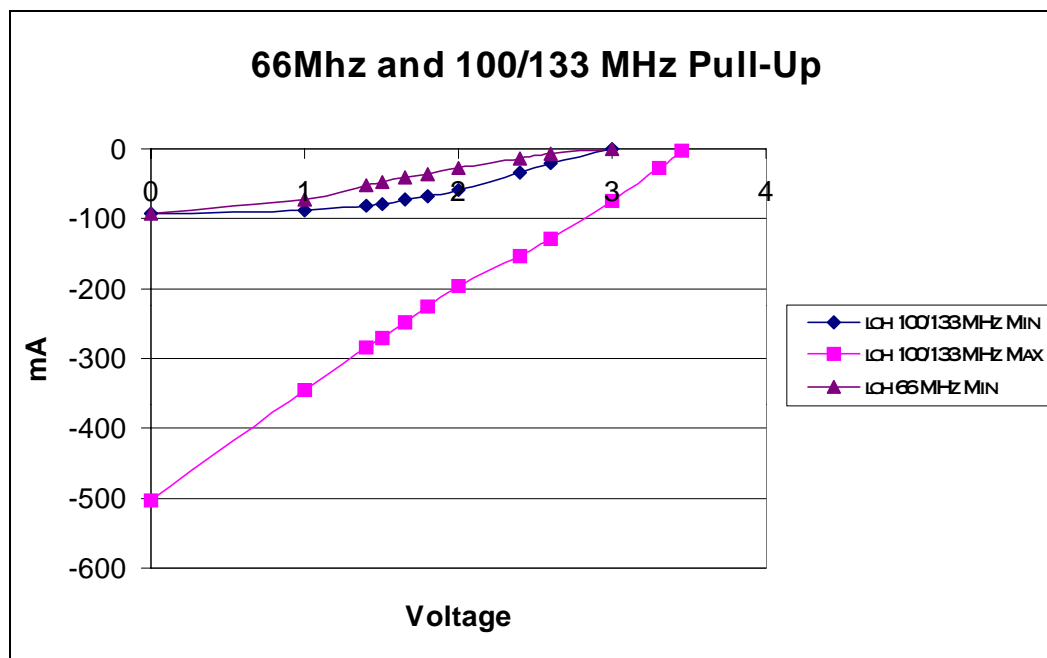
NOTES:

1. Must meet the temperature and voltage range specified above.
2. This drawing is not to scale. Comparisons should be made to the data table provided.

Table 11. Data Points For Figure 4

Pulldown			
Voltage (V)	I (ma)	I (ma)	I (ma)
	100/133MHz min	100/133MHz Max	66 MHz min
0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3	80.3	219.6	54.2
3.45	81.4	222.6	54.9

Figure 5. SDRAM DQ Output Buffer Pull-Up Characteristics (Vcc= 3.0-3.45V)



NOTES:

1. Must meet the temperature and voltage range specified above.
2. This drawing is not to scale. Comparisons should be made to the data table provided.

Table 12. Data Points For Figure 5

Pullup			
Voltage	100/133 MHz min	100/133 MHz max	66 MHz min
(V)	I(ma)	I(ma)	I(ma)
3.45		-2.4	
3.3		-27.3	
3	0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2	-58.7	-197	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73	-248	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1	-88.6	-344.5	-72.5
0	-93	-502.4	-93

3.2 Device Parasitic validation

Device parasitics capacitance is characterized for all input pins, I/O pins and clock pins. The test conditions and specification limits are summarized in [Table 13](#).

The device parasitic capacitance is characterized with a HP capacitance meter (Max freq. > 1Mhz). DUT is interfaced to the test probe through specially designed test fixture to allow ease of probing. The measurement is done under the specified conditions listed in [Table 13](#). The parasitic capacitance introduced by the test fixture is characterized and extracted from the final results.

Table 13. Parasitic capacitance tests

Symbol	Parameter	Condition	Min	Max	Units	Notes
Cin	Input Pin Capacitance	@ 1 MHz, 23°C Tj, 1.4v bias, 200mv swing, Vcc=3.3v	2.5	3.8	pF	Target 3.15pf
CI/O	I/O Pin Capacitance	@ 1 MHz, 23°C Tj, 1.4v bias, 200mv swing, Vcc=3.3v	4.0	6.5	pF	Target 4.8pf
Cclk	Pin Capacitance	@ 1 MHz, 23°C Tj, 1.4v bias, 200mv swing, Vcc=3.3v	2.5	3.5	pF	Target 3.0pf

4.0 System Level Validation of SO-DIMM Modules

SO-DIMM module's functionality and compatibility are tested on Intel reference platforms with industry standard and Intel specific test software. The test conditions are specified in [Section 2.2](#), "SO-DIMM System tests" on [page 5](#). SO-DIMM modules must be assembled with validated PC133 SDRAM components as listed on Intel web page: <http://developer.intel.com/technology/memory/pc133sdr/valid/pc133sdr.htm>

System level validation consists of memory SPD check, memory power up test (power cycling), power management test (S3) and functionality test.

4.1 SO-DIMM validation process and sample requirement

4.1.1 Validation process

Intel has qualified and set up third party test lab(s) for validation. The test lab information is listed at <http://developer.intel.com/technology/memory/pcsdram>. The memory suppliers will initiate the validation process by contacting the preferred validation lab and reaching all the agreements with test labs directly. Validation samples should be submitted to the test lab by closely following the Intel procedure (see sample requirement and shipping instructions in [Section 4.1.1](#)). Once the validation lab receives the validation samples, validation procedures will be carried out as documented in [Section 4.2](#). The validation results will be sent to Intel upon test completion, with

supplier consent, for data review. Once Intel determines all test procedures are correct and the test results pass the success criteria, Intel will post the validation result on the Intel PC133 validation page <http://developer.intel.com/technology/memory/pcsdram/>. If Intel concludes a failure with the validation, the result will be communicated to the supplier. New samples may be submitted for validation once the failure is root caused and fixed. For a more detailed description of the validation process and download of other collaterals, please visit <http://developer.intel.com/technology/memory/pcsdram/>.

4.1.2 Validation sample requirement

Ten (10) PC133 SO-DIMMs are required for validation. The SO-DIMMs must be built with Intel validated PC133 DRAMs as listed at Intel web page: <http://developer.intel.com/technology/memory/pc133sdram/valid/pc133sdram.htm>. The SO-DIMMs must also pass the supplier internal testing and quality control process. A hard copy of “SO-DIMM validation compliance sheet” is required to be included with the sample shipment and a soft version to be emailed to the validation lab and Intel.

4.2 SO-DIMM validation test flow

SO-DIMM validation tests are run in the sequence as specified in the table below.

Table 14. Validation test flow

Sequence	Tests
1	SPD check
2	Power cycling test
3	Power management test
4	Functionality test (short test)
5	Functionality test (four corner test)

4.2.1 Memory SPD check

The purpose of memory SPD check is to confirm the SO-DIMM SPD programming is compliant to Intel SPD specification. The SO-DIMM content is dumped out and compared to Intel specification. Any deviation from Intel specification constitutes a failure.

4.2.2 Power cycling test

The purpose of this test is to insure memory power up sequence is correct and no memory related issue to prevent system from successful booting up and shutting down. The reference platform with SO-DIMM under test is repeatedly powered down and then powered up. Any problem to boot up to designated OS or shut down completely constitutes a failure.

4.2.3 Power management test

The purpose of this test is to insure the system is able to enter and exit respective power management modes successfully. For Intel mobile chipset based platform, only S3 mode is tested. The S3 mode is initiated by software and exited by a keyboard action. Any problem to enter or exit the S3 state is recorded as a failure.

4.2.4 Functionality test

The purpose of this test is to examine the system memory functionality for correct operation under stressed conditions. System memory functionality is tested by checking the memory read and write accuracy with different data patterns, data lengths, address schemes and read/write algorithm at Vcc and temperature specification limits.

Functional test is run for 24 hours under the 4 corner conditions as specified in [Table 15](#)

Table 15. Four coner test conditions

Corner	Vcc	Ambient temperature	System loading
1	3.0V	55C	Heavy/light in X-X config
2	3.6V	55C	Heavy/light in X-X config
3	3.0V	25C	Heavy/light in X-X config
4	3.6V	25C	Heavy/light in X-X config

Xlinear, Mstress and walk01 software are used to perform the functional test.

4.2.4.1 Xlinear test

Xlinear is an Intel proprietary software developed to perform Memory read and Memory write with varying data lengths, data patterns, segment sizes, block sizes and different target locations. It fills a desire data patterns into the desire Memory location and verifies each address for a correct data pattern.

Memory cycle read & write test:

Memory write and read of 14 different patterns is performed in 64K segments of 32-bit, 16-bit, 8-bit and 4-bit widths. With each segment and block size, a pattern is first written to a 64k cache buffer, then transferred back to the memory in one burst cycle, and finally compared for correctness with the original pattern. The same operation is repeated until the full range of memory is tested.

Segment and block test

Memory write and read of multiple patterns is performed in varying segment and block sizes of 32-bit, 16-bit, 8-bit and 4-bit widths. The starting segment is set to 4k and block size 8k. With each segment, a pattern is first written to the cache buffer, then transferred back to the memory in one burst cycle, and finally compared for correctness with the original pattern. The segment and block sizes are subsequently doubled to continue the same test until the segment size reaches 4M and block size reaches 8M.

Back-to-back

Single 32-bit and 16-bit words are written to the cache and then transferred back to the memory. The pattern is subsequently compared for correctness with the original pattern.

Random data test

600 random patterns of 64K segments, one at a time, are written to the full range of memory and then read back to compare for correctness.

Random address test

Multiple patterns of 64K segments, one at a time, are written to the full range of memory and then read back in 25 random address combinations to compare with the original pattern for correctness.

4.2.4.2 Mstress test

Mstress performs memory read and write tests by filling desired data patterns to desired memory locations and verifies each address location for a correct data patterns. It also deploys a set of patterns that generates a high-level of bus noise and utilizes some very unique read/write algorithms to stress the memory read and write functionality. It can be run only under “bare” DOS session, i.e. without any memory manager. This test was originally developed by a Russian computer engineer then refined by Intel.

4.2.4.3 Walk01

Walk01 software is designed to catch any glitch that may occur on the data bus by walking a zero bit while all other bits remain high. It walks a 32 bit field at a time, starting from the lower 32-bit then moving on to the upper 32-bit field. The program reads the command line argument to determine the number of block size and the offset address to be tested. If any glitch occurs within the valid data window, the program will halt for error notification.

Appendix A

DRAM Output Load Specification

Access times for 66 MHz, 100 MHz and 133MHz SDRAM devices are specified into a 50pf load only, without resistive termination.

Applications which are being simulated and implemented *do not* have a resistive termination.

Both Tac and Toh specifications are simulated based on the following:

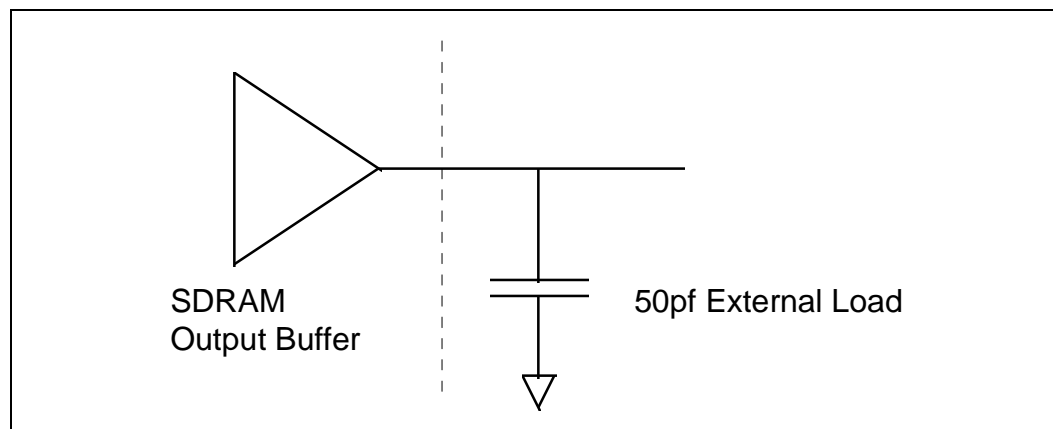
	66 MHz	100 MHz	133 MHz	Load
Tac	9ns	6ns	5.4ns	50pf
Toh	3ns	3ns	3ns	50pf

NOTES:

1. @ Vcc= 3.0v to 3.6v
2. @ Ta= 0C to 65C

If test conditions other than 50pf capacitive load are used, then the proper correlation factor should be used for your specific test condition.

Figure 6. Output Load Circuit



Appendix B

HP83K F330 Tester Correction Factor Study for DRAM AC Timing

Background

PC SDRAM Specification states the following for AC timing at 133Mhz:

$T_{ac} = 5.4 \text{ ns @ } 50\text{pf}; \text{ or } 4.6 \text{ ns @ } 0\text{pf}$

$T_{oh} = 3.0 \text{ ns @ } 50\text{pf}; \text{ or } 1.8 \text{ ns @ } 0\text{pf}$

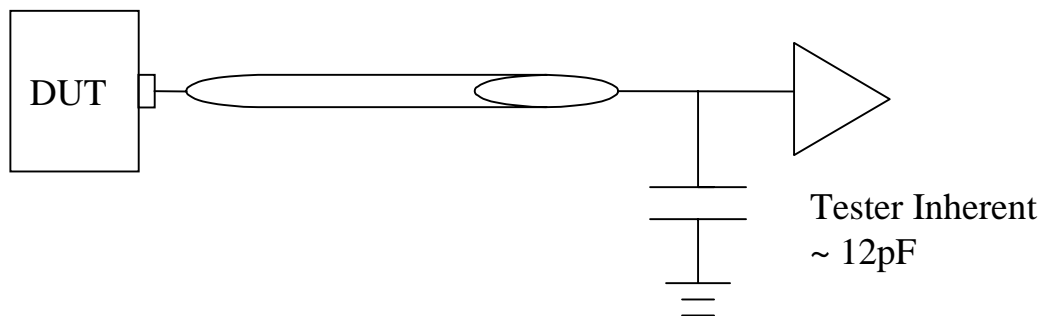
T_{ac} and T_{oh} can be measured using a HP83K F330 Tester. However, the tester environment has about 12pf of total loading capacitance. The measured data need to be corrected to be interpreted at 50pf. This document details the methods and data collected in order to determine the tester correction factors.

Experiment

A 64Mbit (8Mx8) 133Mhz device was soldered down on a Ideal Logic SMT002-01A load board. AC timing was measured with device looping in read cycle.

First, HP83000F330 tester was used to measure T_{ac} and T_{oh} using binary search. An auto calibration routine was performed to calibrate out the intrinsic parasitic effect resulted from the load board, socket and transmission lines. Therefore, the AC timing measured by HP83K is only affected by a total capacitance load of 12pf from the tester comparator. The tester comparator is set at 1.5V. The test set up is illustrated in Figure 1.

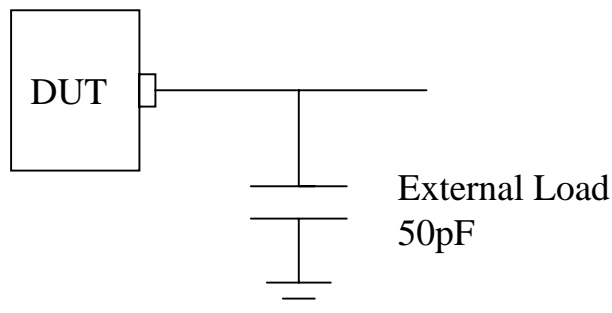
Figure 1. HP 83K F330 Test Set Up



Then, the AC timing of the same device was measured using a Tektronix TDS784 oscilloscope and active probes P6245 without any external capacitance. The trace capacitance on this set up, which included the active probes, the jumper and the transmission lines, is approximately 13pf.

The measurements on the scope were repeated by adding an external capacitance of 50pf. The test set up is illustrated in Figure 2.

Figure 2. Oscilloscope Test Set Up



Experimental Data

The AC timing data for 4 pins at room temperature, 3.3V Vcc are listed in Table 1.

Table 1. AC timing data

	Oscilloscope				HP83K F330	
	load: trace cap		load: trace+50pf		load: 12pf	
Pin	Tac (ns)	Toh (ns)	Tac (ns)	Toh (ns)	Tac (ns)	Toh (ns)
DQ0	4.3	4.1	5.2	4.8	4.11	3.93
DQ3	4	3.8	4.9	4.6	3.92	3.56
DQ4	3.9	3.8	4.9	4.6	3.92	3.58
DQ7	4.3	4	5.1	5	4.08	3.65

Data Analysis and Results

Under the setup conditions in this experiment, AC timing has a linear relationship with the capacitance load. This can be derived mathematically:

$$V = V_{oe}^{-t/RC}$$

V, Vo and R are held constant \Rightarrow

$$t \propto RC$$

$$\Delta t \propto \Delta C$$

Since the device was tested at 12pf on HP83K, to interpret the values at 50pf the following correction factors are computed:

$$T_{ac} = +0.7ns$$

$$T_{oh} = +0.6ns$$

As a result, the HP83K measured data should be corrected as shown in Table 2:

Table 2. Measured vs. Interpreted Value

Pin	HP83K Measured		Interpreted @ 50pf	
	Tac (ns)	Toh (ns)	Tac (ns)	Toh (ns)
DQ0	4.11	3.93	4.81	4.53
DQ3	3.92	3.56	4.62	4.16
DQ4	3.92	3.58	4.62	4.18
DQ7	4.08	3.65	4.78	4.25